REMARKS

Applicants respectfully request reconsideration of the present application in view of the reasons that follow.

Status of Claims:

No claims are currently being added, cancelled or amended.

A detailed listing of all claims that are, or were, in the application, irrespective of whether the claims remain under examination in the application, is presented, with an appropriate defined status identifier.

Claims 1-19 remain pending in this application.

Claim Rejections – Prior Art:

In the final Office Action, claims 1-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,630,056 to Horvath et al. in view of EP Publication No. 0747803 to Meyers et al. This rejection is traversed for at least the reasons given below.

Independent claim 1 recites, among other things:

wherein each of said reception interface sections includes a communication error processing section which, upon occurrence of an error in said received data by one of said reception interface sections, stops receiving said data, sends a communication error signal to all other of said reception interface sections to stop data reception from said data sender, and requests said data sender to resend data,

wherein each of said reception interface sections includes an arithmetic operation unit, an I/O unit, and a memory bridge that provides data from said arithmetic operation unit to said I/O unit of the respective reception interface section,

wherein said error in said received data is detected by said memory bridge of said one of said reception interface sections, and

wherein said memory bridge of said one of said reception interface sections sends the communication error signal to said other memory bridges of said other reception interface sections.

Turning now to the cited art of record, Horvath teaches parallel processing, which enables concurrently processing information received from a data source (in this case a bus). The parallel processing can provide identical processing of data. However, Horvath does not teach or suggest a plurality of reception interface sections that each includes an arithmetic operation unit, an I/O unit, and a memory bridge that provides data from said arithmetic

operation unit to said I/O unit of the respective reception interface section. Further, Horvath does not teach or suggest that an error in the received data is detected by the memory bridge of one of reception interface sections, and that the memory bridge that detected the communication error notifies the memory bridges of the other reception interface sections of the communication error.

The final Office Action appears to recognize these deficiencies of Horvath, and cites Meyers for allegedly teaching these features missing in Horvath. However, this assertion is incorrect. Namely, Meyers does not teach or suggest that a memory bridge of one reception interface section notifies the memory bridges of the other reception interface sections of the communication error. Rather, a state machine of one interface unit 24a notifies another interface unit 24b of a lost sync error signal, whereby a state machine clearly does not correspond in any way, shape or form to a memory bridge that provides data from an arithmetic operation unit to an I/O unit of a reception interface unit.

Still further, the final Office Action incorrectly asserts that Meyers teaches the sending of an error message from one reception interface section to all other reception interface sections. Rather page 14, lines 1-28 of Meyers merely describes that both interface units 24a, 24b assemble the same message packets for transmission from X and Y ports, whereby the message packet being transmitted by the interface unit 24b is also coupled to the other interface unit 24a for cross-checking for errors. Thus, it is not a communication error signal that is sent by a reception interface section (e.g., 24b) in the system of Meyers, but rather a message packet itself that is sent to another reception interface section (e.g., 24a) in the system of Meyers, whereby that other reception interface section then does a comparison with its own received message packet to see if they coincide, and if not, a lock-step error is deemed to have occurred.

Also, the reception interface sections 24a, 24b in Meyers correspond to I/O units, and are not units that provide for data transfer between an I/O unit and an arithmetic operation unit, as clearly seen from a review of Figures 6 and 8 of Meyers.

Accordingly, presently pending independent claim 1, as well as presently pending independent claims 7 and 12 that recite similar features, are patentable over the cited art of record.

Still further, with respect to dependent claims 17-19, those claims recite that the communication error signal is sent from one memory bridge to the other memory bridges as an open drain signal, as described, for example, on page 9, lines 3-4 of the specification.

In its rejection of claims 17-19, the final Office Action asserts that Figures 5 and 10 and page 19, lines 34-54 of Meyers teach the features recited in these claims, but this assertion is incorrect. Namely, page 19, lines 34-54 of Meyers describes that each memory interface 70 receives 64 bits of data to be written to memory, and transfers a portion of the 64 bits of data to the other for cross-checking between them. This portion of Meyers also describes that error-checking is performed on read operations by ECC check circuits 85 of each memory interface 70, whereby an error signal is issued when an uncorrectable error is detected. Nowhere in this portion of Meyers, and nowhere in Figures 5 and 10 of Meyers, is there any teaching of the use of an open-drain signal to send error messages between the memory interfaces 70.

Accordingly, claims 17-19 are patentable for these additional reasons, beyond the reasons given above for their respective base claims.

Conclusion:

Since all of the issues raised in the final Office Action have been addressed in this Amendment and Reply, Applicants believe that the present application is now in condition for allowance, and an early indication of allowance is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing or a credit card payment form being unsigned, providing incorrect information resulting in a rejected credit card transaction, or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. §1.136 and authorize payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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